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EXAMINER	
HU, RUI MENG	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/830,117	TSAI ET AL.	
	Examiner	Art Unit	
	RuiMeng Hu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-92* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :4/21/2004, 1/10/2005, 1/21/2005.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19, 38, 54, 73, 92 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The use of *"protocols"* or "*standards"*, protocols and standards change over time, hence, it is inappropriate to have the scope of a claim change with time. Since organizations implementing standards meet regularly and have the authority to modify standards, any connection a claim may have to these standards may varying scope over time. The other aspect arising from this is enablement. If the standard changes, the disclosure may no longer support the limitation. The scope of the invention sought to be patented cannot be determined from the language of the claims, thus claims 19, 38, 54, 73, 92 are rejected under 35 U.S.C. 112, second paragraph.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14, 16-18, 20-33, 35-37, 39-49, 51-53 are rejected under 35 U.S.C. 102(b) as being anticipated by **Gabara (US Patent 6307443 B1).**

Consider **claim 1**, Gabara clearly discloses a filter calibration circuit (figure 1), comprising: a comparator (figure 1, monitoring circuit 34 compares the magnitude of a current input from detector circuit 20 with the magnitude of a previous input and produces an output signal 38 which indicates the results of the comparison, column 2 line 53-column 3 line 35) operable to generate a comparator output based on a filter output amplitude signal (figure 1, an output 16) and a reference amplitude signal (magnitude of a previous input signal), the filter output amplitude signal (figure 1, signal 28) corresponding to an amplitude of an output signal produced by a filter circuit (filter 12) that is to be calibrated to a desired frequency; and a calibration logic unit (figure 1, tuning circuit 30) operable to receive the comparator output and produce a component code (one or more signal components, or component code for adjusting digitally tunable capacitor array filter, column 4 lines 1-9) to be used by the filter circuit in adjusting one or more component values in the filter circuit.

Consider **claim 20**, Gabara clearly discloses a filter calibration circuit (column 2 line 53-column 3 line 35), comprising: comparing means (monitoring circuit 34 compares) for generating a comparator output based on a filter output amplitude signal (magnitude of current input) and a reference amplitude signal (magnitude of previous input), the filter output amplitude signal corresponding to an amplitude of an output signal produced by a filtering means that is to be calibrated to a desired frequency

(figure 1, signal 28); and code generating means (figure 1, FSM 36) for receiving the comparator output and producing a component code to be used by the filtering means in adjusting one or more component values in the filtering means (column 4 lines 1-9, component code for adjusting digitally tunable capacitor array filter).

Consider **claim 39**, Gabara clearly discloses a method for calibrating a filter circuit (column 2 line 53-column 3 line 35), the filter circuit receiving an input signal (figure 1, signal 14) and producing a filtered output signal (signal 16), the method comprising: generating a comparator output (output of monitoring circuit 34) based on a filter output amplitude signal (signal 28) and a reference amplitude signal (magnitude of previous input), the filter output amplitude signal (signal 28) corresponding to an amplitude of the filtered output signal (magnitude of signal 16) at a desired frequency; generating a component code (one or more signal components) based on the comparator output; and adjusting one or more component values in the filter circuit based on the component code (column 4 lines 1-9, component code for adjusting digitally tunable capacitor array filter).

Consider **claim 2 as applied to claim 1**, **claim 21 as applied to claim 20, claim 40 as applied to claim 39**, Gabara clearly discloses further comprising: an amplitude detector (figure 1, detector 20) operable to receive the filter circuit output signal (signal 16) and generate the filter output amplitude signal (signal 28) based on an amplitude of the filter circuit output signal at the desired frequency.

Consider **claim 3 as applied to claim 1**, **claim 22 as applied to claim 20,** Gabara clearly discloses wherein: the filter circuit includes an LC tank circuit (column 1 lines 26-29).

Consider **claim 4 as applied to claim 1, claim 23 as applied to claim 20**, Gabara clearly discloses wherein: the calibration logic unit includes a digital signal processor (column 1 lines 26-45).

Consider **claim 5 as applied to claim 4**, **claim 24 as applied to claim 23**, Gabara clearly discloses wherein: the digital signal processor includes the comparator (monitoring circuit 34 compares).

Consider **claim 6 as applied to claim 1**, **claim 25 as applied to claim 20**, Gabara clearly discloses wherein: the calibration logic unit includes a logic circuit (column 4 lines 10-19, logical tuning schemes).

Consider **claim 7 as applied to claim 6**, **claim 26 as applied to claim 25**, Gabara clearly discloses wherein: the logic circuit includes the comparator (monitoring circuit 34 compares).

Consider **claim 8 as applied to claim 1**, **claim 27 as applied to claim 20**, Gabara clearly discloses wherein: the component code varies a capacitance in the filter circuit (consider tuning digitally tunable capacitor array filter).

Consider **claim 9 as applied to claim 8**, **claim 28 as applied to claim 27**, Gabara clearly discloses wherein: the capacitance varied is monolithically fabricated on a semiconductor substrate (column 1 lines 9-14).

Consider **claim 10 as applied to claim 8**, **claim 29 as applied to claim 27**, Gabara clearly discloses wherein: the component code varies the capacitance by controlling a number of capacitive elements active in the filter circuit (considering tuning digitally tunable capacitor array filter).

Consider **claim 11 as applied to claim 1**, **claim 30 as applied to claim 20**, Gabara clearly discloses further comprising:

a digital-to-analog converter operable to receive a digital reference amplitude code and produce the reference amplitude signal (column 1 lines 26-45 shows a DC reference voltage can be digitized and stored in DSP, column 3 lines 20-26, the current and previous magnitude signals are stored in the digital memory, if the comparison would be done in analog stage then a digital-to-analog converter is required).

Consider **claim 12 as applied to claim 11**, **claim 31 as applied to claim 30**, Gabara clearly discloses wherein: the calibration logic unit is operable to produce the digital reference amplitude code based on the comparator output (column 1 lines 26-45 shows a DC reference voltage can be digitized and stored in DSP, column 3 lines 20-26, magnitude of previous input is digitized and stored in the digital memory).

Consider **claim 13 as applied to claim 1**, **claim 32 as applied to claim 20**, Gabara clearly discloses further comprising: an analog-to-digital converter operable to receive the filter output amplitude signal and produce a corresponding digital amplitude code (column 3 lines 20-26).

Consider **claim 14 as applied to claim 13**, **claim 33 as applied to claim 32**, Gabara clearly discloses wherein: the comparator is operable to use the digital

amplitude code as the filter output amplitude signal and a stored digital amplitude code as the reference amplitude signal (column 3 lines 20-26).

Consider **claim 16 as applied to claim 1**, **claim 35 as applied to claim 20**, **claim 51 as applied to claim 39,** Gabara clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency automatically when the filter calibration circuit is connected to a power source (when the filter calibration circuit is activated, it is capable of automatically calibrating the filter circuit (figure 3), title).

Consider **claim 17 as applied to claim 1**, **claim 36 as applied to claim 20**, **claim 52 as applied to claim 39,** Gabara clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring a reduction in a quality factor of the filter circuit (varying center frequency not bandwidth, thus a quality factor is maintained (column 3 lines 36-45 figure 2)).

Consider **claim 18 as applied to claim 1**, **claim 37 as applied to claim 20**, **claim 53 as applied to claim 39,** Gabara clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring manual calibration of the filter circuit (according to the particular tuning algorithm (figure 3), title).

Consider **claim 41 as applied to claim 39**, Gabara clearly discloses wherein: generating the component code includes digitally generating the component code (consider generating digital code for tuning digitally tunable capacitor array filter).

Consider **claim 42 as applied to claim 41**, Gabara clearly discloses wherein: generating the comparator output includes digitally generating the comparator output (column 3 lines 20-26).

Consider **claim 43 as applied to claim 39**, Gabara clearly discloses wherein: adjusting one or more component values includes adjusting a capacitance in the filter circuit (consider tuning digitally tunable capacitor array filter).

Consider **claim 44 as applied to claim 43**, Gabara clearly discloses wherein: adjusting a capacitance includes adjusting a capacitance monolithically fabricated on a semiconductor substrate (column 1 lines 9-10, the filter is being fabricated as part of integrated circuits (semiconductor substrate)).

Consider **claim 45 as applied to claim 43**, Gabara clearly discloses wherein: adjusting a capacitance includes controlling a number of capacitive elements active in the filter circuit (consider tuning digitally tunable capacitor array filter).

Consider **claim 46 as applied to claim 39**, Gabara clearly discloses further comprising: producing the reference amplitude signal based on a digital reference amplitude code (column 1 lines 26-45, DC reference voltage is stored on the DSP, column 3 lines 20-26, magnitude of the previous input is stored on the digital memory).

Consider **claim 47 as applied to claim 46**, Gabara clearly discloses further comprising: producing the digital reference amplitude code based on the comparator output (column 3 lines 20-26, magnitude of previous input is produced based on the comparator output).

Consider **claim 48 as applied to claim 39**, Gabara clearly discloses further comprising: producing a digital amplitude code based on the filter output amplitude signal (column 3 lines 20-26).

Consider **claim 49 as applied to claim 48**, Gabara clearly discloses further comprising: using the digital amplitude code as the filter output amplitude signal (column 3 lines 20-26); and using a stored digital amplitude code as the reference amplitude signal (column 3 lines 20-26, magnitude of previous input is stored in the digital memory).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 15, 19, 34, 38, 50, 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gabara (US Patent 6307443).**

Consider **claim 15 as applied to claim 1**, **claim 34 as applied to claim 20, claim 50 as applied to claim 39,** Gabara clearly discloses further comprising: a DC voltage source operable to produce the reference amplitude signal (column 1 lines 26-45 shows a DC reference voltage can be digitized and stored in DSP).

However Gabara fails to disclose a variable-gain amplifier, the calibration logic unit operable to vary a gain of the variable-gain amplifier based on the comparator output.

Official Notice is taken that the teaching of adjusting a variable gain amplifier to achieve a desired output signal level is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as for enhancing output signal quality.

Consider **claim 19 as applied to claim 1**, **claim 38 as applied to claim 20**, **claim 54 as applied to claim 39,** Gabara fails to disclose wherein: the filter calibration circuit is compliant with any of IEEE standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

Official Notice is taken that the teaching of a filter calibration circuit, which is compliant with IEEE standards, is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as to increase the functionality.

Claims 55-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gabara (US Patent 6307443)** in view of **Johnson (US Patent 6766150).**

Consider **claim 55**, Gabara clearly discloses a filter circuit (column 2 line 53-column 3 line 35) operable to filter the input signal and a calibration circuit (figure 1, tuning circuit 30) operable to calibrate the filter circuit (figure 1, filter 12) to a desired frequency, the calibration circuit including, a comparator (figure 1, monitoring circuit 34) operable to generate a comparator output based on a filter output amplitude signal (figure 1, signal 28) and a reference amplitude signal (magnitude of previous input or DC reference voltage), the filter output amplitude signal (signal 28) corresponding to an amplitude of an output signal (figure 1, signal 16) produced by the filter circuit; and a calibration logic unit (figure 1, tuning circuit 30) operable to receive the comparator output (output of monitoring circuit 34) and produce a component code to be used by the filter circuit in adjusting one or more component values in the filter circuit (column 4 lines 1-9, component code for adjusting digitally tunable capacitor array filter).

However, Gabara fails to specifically disclose the filter circuit is for use in transmitter circuit of a wireless transceiver.

In the same field of endeavor, Johnson clearly discloses a system and method

for tuning a narrowband cavity filter used in a CDMA transmitter (figures 3 and 7, Abstract, column 9 lines 12-65).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Johnson into the art of Gabara as to use the filter circuit in a transmitter circuit to pass the desired signal efficiently.

Consider **claim 74**, Gabara clearly discloses a filtering means (figure 1, filter 12, column 2 line 53-column 3 line 35) for filtering the input signal and calibrating means (figure 1, tuning circuit 30) for calibrating the filtering means to a desired frequency, the calibrating means including, comparing means (figure 1, monitoring circuit 34) for generating a comparator output based on a filter output amplitude signal (figure 1, signal 28) and a reference amplitude signal (magnitude of previous input), the filter output amplitude signal (signal 28) corresponding to an amplitude of an output signal (signal 16) produced by the filtering means; and code generating means (figure 1, FSM 36) (column 4 lines 1-9, component code for adjusting digitally tunable capacitor array filter) for receiving the comparator output and producing a component code to be used by the filtering means in adjusting one or more component values in the filtering means.

However, Gabara fails to specifically disclose the filter circuit is for use in transmitter circuit of a wireless transceiver.

In the same field of endeavor, Johnson clearly discloses a system and method for tuning a narrowband cavity filter used in a CDMA transmitter (figures 3 and 7, Abstract, column 9 lines 12-65).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection technique taught by Johnson into the art of Gabara as to use the filter circuit in a transmitter circuit to pass the desired signal efficiently.

Consider **claim 56 as applied to claim 55**, **claim 75 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein the calibration circuit includes: an amplitude detector (figure 1, detector 20) operable to receive the filter circuit output signal and generate the filter output amplitude signal (signal 28) based on an amplitude of the filter circuit output signal at the desired frequency.

Consider **claim 57 as applied to claim 55**, **claim 76 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the filter circuit includes an LC tank circuit (column 1 lines 26-29).

Consider **claim 58 as applied to claim 55**, **claim 77 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the calibration logic unit includes a digital signal processor (column 1 lines 26-45).

Consider **claim 59 as applied to claim 58**, **claim 78 as applied to claim 77,** Gabara as modified by Johnson clearly discloses wherein: the digital signal processor includes the comparator (monitoring circuit 34 compares).

Consider **claim 60 as applied to claim 55**, **claim 79 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the calibration logic unit includes a logic circuit (column 4 lines 10-19, logical tuning schemes).

Consider **claim 61 as applied to claim 60**, **claim 80 as applied to claim 79,** Gabara as modified by Johnson clearly discloses wherein: the logic circuit includes the comparator (monitoring circuit 34 compares).

Consider **claim 62 as applied to claim 55**, **claim 81 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the Component code varies a capacitance in the filter circuit (considering tuning digitally tunable capacitor array filter).

Consider **claim 63 as applied to claim 62**, **claim 82 as applied to claim 81,** Gabara as modified by Johnson clearly discloses wherein: the capacitance varied is monolithically fabricated on a semiconductor substrate (column 1 lines 9-14, integrated circuits).

Consider **claim 64 as applied to claim 62**, **claim 83 as applied to claim 81,** Gabara as modified by Johnson clearly discloses wherein: the component code varies the capacitance by controlling a number of capacitive elements active in the filter circuit (consider tuning digitally tunable capacitor array filter).

Consider **claim 65 as applied to claim 55**, **claim 84 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein the calibration circuit includes: a digital-to-analog converter operable to receive a digital reference amplitude code and produce the reference amplitude signal (column 1 lines 26-45 shows a DC reference voltage can be digitized and stored in DSP, column 3 lines 20-26, the current and previous magnitude signals are stored in the digital memory, if the comparison would be done in analog stage then a digital-to-analog converter is required).

Consider **claim 66 as applied to claim 65**, **claim 85 as applied to claim 84,** Gabara as modified by Johnson clearly discloses wherein: the calibration logic unit is operable to produce the digital reference amplitude code based on the comparator output (column 1 lines 26-45 shows a DC reference voltage can be digitized and stored in DSP, column 3 lines 20-26, magnitude of previous input is digitized and stored in the digital memory).

Consider **claim 67 as applied to claim 55**, **claim 86 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein the calibration circuit includes: an analog-to-digital converter operable to receive the filter output amplitude signal and produce a corresponding digital amplitude code (column 3 lines 20-26).

Consider **claim 68 as applied to claim 67**, **claim 87 as applied to claim 86,** Gabara as modified by Johnson clearly discloses wherein: the comparator is operable to use the digital amplitude code as the filter output amplitude signal and a stored digital amplitude code as the reference amplitude signal (column 3 lines 20-26).

Consider **claim 70 as applied to claim 55**, **claim 89 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the calibration circuit is operable to calibrate the filter circuit to the desired frequency automatically when the calibration circuit is connected to a power source (when the filter calibration circuit is activated, it is capable of automatically calibrating the filter circuit (figure 3), title).

Consider **claim 71 as applied to claim 55**, **claim 90 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring a

reduction in a quality factor of the filter circuit (varying center frequency not bandwidth, thus a quality factor is maintained (column 3 lines 36-45 figure 2)).

Consider **claim 72 as applied to claim 55**, **claim 91 as applied to claim 74,** Gabara as modified by Johnson clearly discloses wherein: the calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring manual calibration of the filter circuit (according to the particular tuning algorithm (figure 3), title).

Consider **claim 69 as applied to claim 55**, **claim 88 as applied to claim 74,** Gabara as modified by Johnson clearly discloses further comprising: a DC voltage source operable to produce the reference amplitude signal (column 1 lines 26-45 shows a DC reference voltage can be digitized and stored in DSP).

However Gabara fails to disclose a variable-gain amplifier, the calibration logic unit operable to vary a gain of the variable-gain amplifier based on the comparator output.

Official Notice is taken that the teaching of adjusting a variable gain amplifier to achieve a desired output signal level is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as for enhancing output signal quality.

Consider **claim 73 as applied to claim 55, claim 92 as applied to claim 74,** Gabara as modified by Johnson fails to disclose wherein: the filter calibration circuit is compliant with any of IEEE standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

Official Notice is taken that the teaching of a filter calibration circuit, which is compliant with IEEE standards, is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as to increase the functionality.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to:**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RuiMeng Hu whose telephone number is 571-270-1105. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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RuiMeng Hu
R.H./rh
June 5, 2007

EDAN ORGAD
PRIMARY PATENT EXAMINER
6/6/07